In re Patent Application of
RAYNOR
Serial No. 10/786,878
Filed: FEBRUARY 25, 2004

REMARKS

Applicant thanks the Examiner for the careful and thorough examination of the present application. Applicant submits that all claims are patentable and presents arguments below supporting such patentability.

I. The Claimed Invention

Independent Claim 11 is directed to an image sensing structure including a photodiode comprising a layer comprising a first conductivity type epitaxial layer and having an upper surface, and a well of a second conductivity type having opposing sides and positioned in the layer. The well defines a collection node. The photodiode further comprises an isolation trench at least partially bounding an upper portion of the well at the opposing sides thereof and comprising a shallow trench isolation (STI) having a depth from the upper surface of the layer less than the depth of the well. The epitaxial layer provides increased sensitivity of the photodiode, as disclosed in the present application. (Specification of present application, ¶ 25).

Independent Claim 20 is directed to a CMOS image sensing structure similar to independent Claim 11. Independent Claim 37 is directed to an image sensing structure similar to independent Claim 11, without the epitaxial recitation, and further recites an n-p junction formed at an interface between the STI and the well, and an STI width substantially extending over the width of the pixel.

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II. The Claims Are Patentable

The Examiner rejected independent Claims 11, 20, and 37 over Yang in view of Rhodes. The Yang patent discloses a photodiode with a layer of a first conductivity type positioned between an oxide-rich silicon layer 56, a depletion region 54, and a doped region 52. (Figure 2). The Examiner correctly notes that Yang fails to teach a layer comprising a first conductivity type epitaxial layer and having an upper surface, as recited in independent Claims 11 and 20. The Examiner looked to Rhodes to supply the noted deficiency.

Rhodes discloses a CMOS imaging circuit that includes a photogate and readout circuit. (Col. 2, lines 38-46). The CMOS imaging circuit comprises an epitaxial silicon layer disposed over an entire wafer. (Col. 7, lines 30-34). The Examiner's stated motivation to combine the epitaxial layer of Rhodes into the photodiode of Yang is to reduce power consumption and form regions/junctions in the base semiconductor structure.

Applicant submits that the Examiner's combination is improper. The Examiner contended that a person of ordinary skill in the art would modify Yang as proposed to reduce power consumption, citing column 1, lines 58-66 of Rhodes. The cited portion of Rhodes recites:

> On-chip integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

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> A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photogate, photoconductor or a photodiode overlying a doped region of a substrate for accumulating photo-generated charge in the underlying portion of the substrate. (Col. 1, lines 58-66).

Rhodes does not teach that forming layers from epitaxy reduces the overall power consumption of the fabricated device. Indeed, Rhodes teaches that CMOS image sensor generally reduces power consumption and not epitaxial layers as contended by the Examiner. (Col. 1, lines 49-63). Accordingly, for this reason alone, independent Claims 11 and 20 are patentable.

Moreover, Applicant submits that Yang and Rhodes are divergent approaches, and, indeed, teach away from their selective combination. Yang teaches shallow trench isolation (STI) structures 48 versus the insulation layer 18, as disclosed in the Background of Invention Section of Yang. Rhodes discloses forming the insulation sidewalls 112 with field oxide, (Col. 8, lines 60-64), rather than with STI structures as taught by Yang. Given that Yang discloses STI structures rather than oxide layers for insulation regions, Applicant submits that the person of ordinary skill in the art would be taught away from combining the two references as proposed. Indeed, as the Examiner correctly notes in his argument, "Yang discloses the STI surrounding the photodiode region and other units to reduce the leakage current" rather than using insulation layers, which are taught as suffering from greater leakage current. (Col. 1, lines 47-55).

Therefore, for this reason also, independent Claims 11, 20, and 37 are patentable.

In the rejection of independent Claim 37, the Examiner contended that the feature of an isolation trench comprising a shallow trench isolation (STI) and having a width substantially extending over the width of the pixel was disclosed by Yang in view of Rhodes. The Examiner contended:

> Yang discloses the STI surrounding the photodiode region and other units to reduce the leakage current (col. 2, lines 1-19) and Rhodes discloses the STI's 112 are formed around a pixel cell 14 (Rhodes col. 8, lines 43-57 and fig. 7). Therefore, Yang and Rhodes both disclose the STI and the photodiode region (n-well) substantially extending over the width of the pixel.

Applicant respectfully submits that the Examiner has mischaracterized Rhodes. As discussed above, Rhodes does not disclose STI structures. Indeed, Rhodes discloses the use of an alternative to STI structures, namely, field oxide insulation regions. Therefore, for this reason also, independent Claim 37 is patentable over the prior art.

Furthermore, in the Examiner's rejection of Claim 37, the Examiner cited Figure 2 of Yang, reproduced below, as disclosing an isolation trench comprising a shallow trench isolation (STI) and having a width substantially extending over the width of the pixel, as recited in Claim 37.

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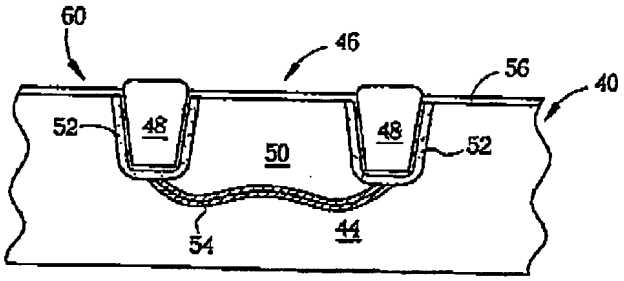

Figure 2 of Yang

Applicant submits that the Examiner has mischaracterized Yang. The conventional STI 48 of Yang does not have a width substantially extending over the width of the pixel 46. Additionally, Applicant submits that the person of ordinary skill in the art would be taught away from such a modification of Yang since the person of ordinary skill in the art would recognize that STIs are used to isolate components. Moreover, since space on the pixel is limited for other components, the person of ordinary skill in the art would be taught away from increasing the size of the STI to substantially extend over the width of the pixel, as in the claimed invention. Therefore, in addition to reasons set forth above, independent Claim 37 is patentable.

Accordingly, it is submitted that independent Claims 11, 20, and 37 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

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CONCLUSIONS

In view of the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,

JACK G. ABID
Reg. No. 58,287
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorney for Applicant

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 23rd day of April, 2007.